Attorney Docket No.: N1085-00209 [TSMC2003-0474]

What is claimed is:

- 1. A single transistor random access memory cell, comprising:
 - a transfer gate; and
- a storage capacitor with a storage node having an MOS native device with a near zero threshold voltage to form an inversion layer.
- 2. The cell as in claim 1, further comprising: an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.
- 3. The cell as in claim 1, wherein:
- a doping profile of the transfer gate and a doping profile of the storage capacitor are substantially the same or are substantially different.
- 4. The cell as in claim 1, wherein the transfer gate and a capacitor plate being closer together than a minimum line width of a single photomask.
- The cell as in claim 4, further comprising:a dielectric spacer between the transfer gate and the capacitor plate.
- The cell as in claim 1, further comprising:

 a shallow trench isolation, STI, insulator having a reduced step height below that of an

 OD sidewall of a substrate insulator; and
 - a capacitor plate covering the STI insulator and the OD sidewall.
- 7. The cell as in claim 6, further comprising:
 an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.
- 8. The cell as in claim 6, wherein the transfer gate has another MOS native device forming an inversion region at a near zero threshold voltage.
- 9. The cell as in claim 6, wherein the transfer gate and a capacitor plate being closer together than a minimum line width of a single photomask.

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- 10. The cell as in claim 6, further comprising:a dielectric spacer between the transfer gate and the capacitor plate.
- 11. The cell as in claim 1, further comprising:a shallow trench isolation, STI, insulator having a reduced step height below that of anOD sidewall of a substrate insulator;

the transfer gate and the capacitor being in an active area of the substrate; an external MOS native device external to the active area, the external MOS native device forming an inversion layer at near zero threshold voltage; and a capacitor plate covering the STI insulator and the external MOS native device.

- 12. The cell as in claim 11, further comprising:
 an inversion region beneath the transfer gate, which is formed by diffusion of the inversion layer.
- 13. The cell as in claim 11, further comprising:
 the transfer gate having an MOS native device forming an inversion region at a near zero threshold voltage.
- 14. The cell as in claim 11, further comprising:
 the transfer gate and a capacitor plate being closer together than a minimum line width of a single photomask.
- 15. The cell as in claim 14, further comprising: a dielectric spacer between the transfer gate and the capacitor plate.
- 16. A method of making a single transistor random access memory cell, comprising: forming a substrate in an active area and an isolation region in the substrate;

forming a transfer gate and forming an electrode plate of a capacitor over the substrate in the active area, with the electrode plate covering a portion of the isolation region;

forming beneath the electrode plate a capacitor storage node that becomes an inversion layer at a near zero threshold voltage without a junction storage node; and

forming an inversion region beneath the transfer gate without a P/N junction.

17. The method of claim 16 wherein, forming the inversion region beneath the transfer gate is by diffusion of the inversion layer.

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18. The method of claim 16 wherein, forming the inversion region beneath the transfer gate is by forming beneath the transfer gate a doped region that becomes an inversion layer at a near zero threshold voltage.

19. The method as in claim 16, further comprising:

forming the transfer gate by a photomask and photo etch process that does not form the electrode plate; and

forming the electrode plate by a photomask and photo etch process that does not form the transfer gate.

- 20. The method of claim 16 wherein, forming the inversion region beneath the transfer gate is by diffusion of the inversion layer.
- 21. The method of claim 16 wherein, forming the inversion region beneath the transfer gate is by forming beneath the transfer gate a doped region that becomes an inversion layer at a near zero threshold voltage.
- 22. The method of claim 16, further comprising:

 recessing a portion of the isolation region lower than a sidewall of the substrate; and covering the sidewall and the portion of the isolation region.
- 23. The method of claim 22 wherein, forming the inversion region beneath the transfer gate is by diffusion of the inversion layer.
- 24. The method of claim 22 wherein, forming the inversion region beneath the transfer gate is by forming beneath the transfer gate a doped region that becomes an inversion layer at a near zero threshold voltage.
- 25. The method as in claim 22, further comprising:

forming the transfer gate by a photomask and photo etch process that does not form the electrode plate; and

forming the electrode plate by a photomask and photo etch process that does not form the transfer gate.

26. The method of claim 16, further comprising:

forming an external doped region external to the active area; and covering the isolation region and the external doped region with the electrode plate.

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- 27. The method of claim 26 wherein, forming the inversion region beneath the transfer gate is by diffusion of the inversion layer.
- 28. The method of claim 26 wherein, forming the inversion region beneath the transfer gate is by forming beneath the transfer gate a doped region that becomes an inversion layer at a near zero threshold voltage.
- 29. The method as in claim 26, further comprising:

forming the transfer gate by a photomask and photo etch process that does not form the electrode plate; and

forming the electrode plate by a photomask and photo etch process that does not form the transfer gate.